Electronic Version
Stylesheet Version v1.1.1

# Description

# AMPLIFIER WITH FIXED INPUT IMPEDANCE OPERATED IN VARIOUS GAIN MODES

## BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to an amplifier with substantially fixed input impedance and related method, and more particularly, to an amplifierand related method for utilizing a plurality of resistive negative feedback circuits to process a plurality of feedback signals so as to keep the input impedance of the amplifier substantially fixed in various gain modes.

[0003] 2. Description of the Prior Art

[0004] Low-noise amplifiers (LNA) are indispensable elements in a receiver of a wireless communications system and used for providing signals received by an antenna with gains and sensitivity. Since the low-noise amplifier is installed

in a front end of the receiver to process generally very weak signals, the performances of the low-noise amplifier, such as the noise figure, the RF gain, and the non-linearity, are highly related to the gross performance of receiver.

[0005] Please refer to Fig.1, which is a functional block diagram of a receiver 10 in a wireless communications system. The receiver 10 in the present embodiment is mainly applied to the wireless communications system operating at 0.9GHz to 10GHz. Nowadays, most commercial wireless communications systems, such as GSM, Blue-tooth, and WLAN, operate around the frequency region (0.9GHz to 10GHz). The receiver 10 includes an antenna 12, a filter 14, a low-noise amplifier 16, a mixer 18, a local oscillator generator 20, and a signal processing module 22. The antenna 12 is used to receive an RF signal RF. After the RF signal RF is obtained from the antenna 12, the filter 14 will operate a frequency selection process for the RF signal RF to generate an input signal SI. The low-noise amplifier 16 then amplifies the input signal SI by a predetermined gain ratio. Since the receivedRF signal RF and the filtered input signal SI are very weak, the low-noise amplifier 16 installed after the filter 14 should bring very low

noise. Afterwards, the input signal SI is outputted from the low-noise amplifier 16 and down-sampled to a specific frequency by the mixer 18 and the local oscillator generator 20. The signal processing module 22 will proceed with advanced operations such as demodulation.

[0006] When being implemented, under various conditions, the receiver 10 of the wireless communications system cannot receive the RF signal RF with fixed magnitude. Taking the signal transmission in a cellular phone as an instance, when the receiver 10 approaches the signal emitting end, such as a base station, the magnitude of the RF signal RF is higher than that when the receiver 10 is far away from the signal emitting end. Since the exceeding RF signal RF may saturate the system and disable the amplifier to linearly amplify signals, the low-noise amplifier 16 is generally designed as a variable gain amplifier operating in a plurality of gain modes. In the following statement, the variable gain amplifier can operate in two gain modes: a high-gain mode and a low-gain mode. As shown in Fig.1, when the input signal SI is small, the low-noise amplifier 16 operates in the high-gain mode, and the input signal SI is amplified by a higher gain ratio and then outputted. On the other hand, when the input signal SI is large, the

low-gain mode is applied to process the input signal SI for avoiding the saturation of the low-noise amplifier 16. Please refer to Fig.2, which is a functional block diagram of an embodiment of the prior-art low-noise amplifier 16 shown in Fig.1. The low-noise amplifier 16 is a variable gain amplifier, which can operate respectively in a high-gain mode and a low-gain mode. The low-noise amplifier 16 includes an input port 32, a gain circuit 34, and an output port 36. The input port 32 is used to receive the input signal SI, and the gain circuit 34 includes transistors Q1-Q5 and adjustable three biases B1-B3. The gain circuit 34 can be used to amplify the input signal SI by two corresponding (high/low) gain ratios respectively in the two (high/low) gain modes. The output port 36 is used to output the input signal SI amplified by the gain circuit 34.

[0007] Please continue to refer to Fig.2. When the low-noise amplifier 16 operates in the high-gain mode, the bias B2 is higher than the bias B3, the transistors Q1, Q2, Q4, Q5 turn on, and the transistor Q3 turns off. The input signal SI is amplified through the transistors Q1, Q2, Q4, Q5 in the gain circuit 34 and outputted by the output port 36. When the low-noise amplifier 16 operates in the low-gain mode, the bias B3 is higher than the bias B2, the transis-

tors Q1, Q3, Q4, Q5 turn on, and the transistor Q2 turns off. The input signal SI is amplified through the transistors Q4, Q5 and outputted by the output port 36. By initially making the sizes of the transistors Q1, Q2, Q3 larger than those of the transistors Q4, Q5, only a little part of the input signal SI passes the transistor Q4, Q5 to the output port 36, while most of the input signal SI passes the transistors Q1, Q3 to a voltage source VCC. Therefore, the switch between the high-gain mode and the low-gain mode relies on the comparison between the bias B2 and the bias B3 with constant bias B1. When being implemented, the bias B2 remains at a predetermined voltage value, while the bias B3 is switched between two values (higher/lower than the bias B2).

[0008] In addition, anamplifier generally includes an input impedance and an output impedance. In a system, once the amplifier is electrically connected to other circuitries, a loading effect may occur to affect the performances of the whole system due to the (input/output) impedance mismatch between the amplifier and other circuitries. Please refer to both Fig.1 and Fig.2. The low-noise amplifier 16 includes an input impedance Zin1, an inductive negative feedback circuit 38, and an inductive loading Lc.

For avoiding the impedance mismatch between the filter 14 and the low-noise amplifier 16 to affect the response of the filter 14 and the performance of the low-noise amplifier 16, in the prior-art embodiment, the emitters of the transistor Q1, Q4 are electrically connected to the inductive negative feedback circuit 38 in order to adjust the input impedance Zin1. Therefore, when the low-noise amplifier 16 is switched between the high-gain mode and the low-gain mode, the response of the filter 14 will not change due to the change of the input impedance Zin1 and thus the performance of the receiver 10 can be maintained.

[0009] However, since the circuit area of the inductive negative feedback circuit 38 is too large, concerning the cost, the resistive loading and the resistive negative feedback circuit are more acceptable for the industry. Please refer to Fig.3, which is a functional block diagram of another embodiment of the prior-art low-noise amplifier 16 shown in Fig.1. The low-noise amplifier 16 is still a variable gain amplifier operating in the high-gain mode and the low-gain mode. Similar to the embodiment shown in Fig.2, the low-noise amplifier 16 consists of the input port 32, the gain circuit 34, the output port 36, and an input

impedance Zin1. The gain circuit 34 includes the transistors Q1-Q5and adjustable three biases B1-B3" for amplifying the input signal SI by corresponding two (high/low) gain ratios respectively in the two (high/low) gain modes. The main difference between the present embodiment and the previous one is that in the present embodiment, a resistive loading RL and a resistive negative feedback circuit 40 substitute the inductive loading Lc and the inductive negative feedback circuit 38 shown in Fig.2 to achieve a negative feedback function. For clarifying the characteristics of the resistive negative feedback, we take another amplifier as an instance. Please refer to Fig.4, which is an (simple) amplifier 50 combined with a resistor Rf used for resistive negative feedback circuit. The amplifier 50 consists of a transistor Q6, an input port 52, an output port 56, an effective resistor R, and a resistor Rf for negative feedback. Without the resistor Rf (for negative feedback) involved, the amplifier has the voltage gain,

$$Av1 = g_m \cdot R$$

wherein $g_m$ is a characteristic parameter of the transistor Q6. As shown in Fig.4, the real line shows a frequency response of the amplifier 50 without the negative feedback (the horizontal axis represents the frequency f, and the vertical axis represents the gain Av). With the resistor Rf involved, the gain diminishes to

$$Av2 \approx g_m \cdot R \cdot Rf /(Rf + R)$$

, and the dotted line shown in Fig.4 represents the frequency response of the amplifier 50 with the negative feedback. As shown in Fig.4, the diminished gain (reduced by

$Rf/(Rf+R))$

) can instead bring a better frequency response for the gain ratio of the frequency response remains flat over a wider frequency range. In the meantime, the distortion is also reduced along with the reduction of the gain ratio. In addition, the input impedance Zin2 of the amplifier 50 is changed to

$$Zin2 \approx (Rf + R)/(g_m \cdot R)$$

by the effect of the resistor Rf; that is, the resistive negative feedback circuit 40 can be used to adjust the input impedance Zin2 of the amplifier.

[0010] Please refer back to Fig.3. The resistive negative feedback circuit 40 is a resistor R electrically connected to a capacitor C. The embodiment shown in Fig.3 operates similarly to the embodiment shown in Fig.2. When the low-noise amplifier 16 operates in the high-gain mode, partial input signal SI processed and outputted to the output port 36 will be fed back from the output port 36 to the input port 32 via the resistive negative feedback circuit 40, called a feedback signal. However, when the low-noise amplifier

16 is switched to the low-gain mode, a little input signal SI will pass the transistors Q4', Q5' to the output port 36, while most of the input signal SI pass the transistors Q1', Q3' to a voltage source VCC'; that is, only a little feedback signal passes the resistive negative feedback circuit 40 back to the input port 32. Therefore, in various gain modes, the resistive negative feedback circuit 40 cannot be used to adjust the input impedance so that the input impedance Zin1' ill alter in different gain modes. As we know, the filtering response of the filter 14 will be distorted by the impedance mismatch between the filter 14 and the low-noise amplifier 16, and the performances of the low-noise amplifier 16 will be affected.

## SUMMARY OF INVENTION

[0011] It is therefore a primary objective of the claimed invention to provide an amplifier and related method for utilizing a plurality of resistive negative feedback circuits to process corresponding feedback signals so as to keep the input impedance of the amplifier substantially fixed in various gain modes and to solve the above-mentioned problems.

[0012] In the amplifier of the claimed invention, a plurality of resistive negative feedback circuits are respectively installed in a plurality of corresponding paths through which a

feedback signal will pass in various gain modes. In each gain mode, at least a corresponding resistive negative feedback circuit will be used to process the corresponding feedback signal, so that the input impedance of the amplifier can remain substantially fixed in various gain modes. In addition, at least a predetermined resistive negative feedback circuit is connected to corresponding switch device for determining whether the feedback signal passes the predetermined resistive negative feedback circuit to the input port according to the corresponding gain mode.

[0013] In the claimed invention, a differential amplifier, operating in a differential mode, is disclosed and achieved by combining two amplifiers of the same characteristics. The differential amplifier of the present invention still has substantially fixed input impedance by utilizing a plurality of resistive negative feedback circuits and at least a corresponding switch device to process the feedback signal in various gain modes, so that the input impedance of the differential amplifier can remain substantially fixed in various gain modes. In addition, with the characteristics of the differential mode, the differential amplifier can stop being interfered with and generating interference while

operating with a wider frequency response.

[0014] According to the claimed invention, an amplifier with substantially fixed input impedance when operating in a plurality of gain modes is disclosed. The amplifier comprises an input port for receiving an input signal, a gain circuit for amplifying the input signal by corresponding gain ratios in various gain modes, a plurality of resistive negative feedback circuits electrically connected to the input port and the gain circuit forkeeping the input impedance of the amplifier substantially fixed in various gain modes, and an output port for outputting the input signal amplified by the gain circuit.

[0015] According to the claimed invention, a method used in an amplifier for keeping the input impedance of the amplifier substantially fixed in a plurality of gain modes is disclosed. The amplifier comprises a gain circuit and a plurality of resistive negative feedback circuits. The method comprises utilizing the gain circuit to switch the amplifier among various gain modes, and utilizing the plurality of resistive negative feedback circuits to keep the input impedance of the amplifier substantially fixed in various gain modes.

[0016] According to the claimed invention, a differential amplifier

with substantially fixed input impedance when operating in a plurality of gain modes comprises: a positive input port for receiving a positive input signal; a negative input port for receiving a negative input signal; a positive amplifier circuit electrically connected to the positive input port, the positive amplifier circuit comprising: a positive gain circuit for amplifying a positive input signal by corresponding gain ratios; and a plurality of positive resistive negative feedback circuits for keeping the input impedance of the positive amplifier circuit substantially fixed in various gain modes; and a negative amplifier circuit electrically connected to the negative input port, the negative amplifier circuit comprising: a negative gain circuit for amplifying a negative input signal by corresponding gain ratios; and a plurality of negative resistive negative feedback circuits for keeping the input impedance of the negative amplifier circuit substantially fixed in various gain modes; a positive output port electrically connected to the positive amplifier circuit for outputting the processed positive input signal; and a negative output port electrically connected to the negative amplifier circuit for outputting the processed negative input signal.

[0017] These and other objectives of the present invention will no

doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the various figures and drawings.

## Brief Description of Drawings

[0018] Fig.1 is a functional block diagram of a receiver in a wireless communications system.

[0019] Fig.2 is a functional block diagram of an embodiment of the prior-art low-noise amplifier shown in Fig.1.

[0020] Fig.3 is a functional block diagram of another embodiment of the prior-art low-noise amplifier shown in Fig.1.

[0021] Fig.4 is an amplifier combined with a resistor Rf used for resistive negative feedback circuit.

[0022] Fig.5 is a schematic diagram of an embodiment of an amplifier according to the present invention.

[0023] Fig.6 is a schematic diagram of another embodiment showing an amplifier according to the present invention.

[0024] Fig.7 is a schematic diagram of a detailed embodiment shown in Fig.6.

[0025] Fig.8 is a list illustrating three biases shown in Fig.7.

[0026] Fig.9 is a flow chart showing a method embodiment according to the present invention.

[0027] Fig.10 is a functional block diagram of a differential amplifier according to the present invention.

[0028] Fig.11 is a schematic diagram of a detailed embodiment of the differential amplifier shown in Fig.10.

## DETAILED DESCRIPTION

[0029] Please refer to Fig.5, which is a schematic diagram of an embodiment of an amplifier 60 according to the present invention. Similar to the prior-art embodiments shown in Fig.2 and Fig.3, the amplifier 60 in the present embodiment includes an input port 62, a gain circuit 64, an output port 66, and an input impedance Zin3. The input port 62 is used to receive an input signal SI3, and the gain circuit 64 includes the transistors Q7-Q11 and three adjustable biases B4-B6. In contrast to the embodiment shown in Fig.2, the transistors Q7-Q11 respectively correspond to the transistors Q1-Q5, and the three biases B4-B6 respectively correspond to the biases B1-B3. The gain circuit 64 is also used to amplify the input signal SI3 received from the input port 62 by corresponding gain ratios in various gain modes. The output port 66 is used to output the input signal SI amplified by the gain circuit 64. The present embodiment inherits the designation of two gain modes (in the prior-art embodiments): a high-gain

mode and a low-gain mode. When the bias B5 is higher than the bias B6, the amplifier 60 operates in the high-gain mode. The input signal SI3 is amplified by the transistors Q7, Q8, Q10, Q11 in the gain circuit 64 and outputted to the output port 66. When the bias B6 is higher than the bias B5, the amplifier 60 operates in the low-gain mode; in the meantime, only a little part of the input signal SI3 will pass the transistors Q10, Q11 to the output port 66, while most of the input signal SI3 will pass the transistors Q7, Q9 to a voltage source VCC. Therefore, in the present embodiment, the switch between the high-gain mode and the low-gain mode is still determined by comparing the bias B5 with the bias B6.

[0030] In each gain mode, a feedback signal will be fed back to the input port via at least a corresponding path. In the present embodiment, the amplifier 60 includes two resistive negative feedback circuits, a high gain resistive negative feedback circuit 67 and a low gain resistive negative feedback circuit 69, which are respectively implemented by a resistor electrically connected to a capacitor (the high gain resistive negative feedback circuit 67 includes a resistor Rf1 and a capacitor Cf1; the low gain resistive negative feedback circuit 69 includes a resistor Rf2 and a ca-

pacitor Cf2). The high gain resistive negative feedback circuit 67 is mainly used to process the feedback signal in the high-gain mode, and the low gain resistive negative feedback circuit 69 is used to process the feedback signal in the low-gain mode. Refer to both the prior-art embodiment shown in Fig.3 and the present embodiment, the high gain resistive negative feedback circuit 67 corresponds to the resistive negative feedback circuit shown in Fig.3; that is, in the high-gain mode, the feedback signal will be fed back form the output port 66 to the input port 62 mainly via the high gain resistive negative feedback circuit 67, while in the low-gain mode, the feedback signal is fed back from the voltage source VCC to the input port 62 mainly via the low gain resistive negative feedback circuit 69. In addition, the amplifier 60 further includes a switch device 68, which is electrically connected to the low gain resistive negative feedback circuit 69. Therefore, when being implemented, in the high-gain mode, the switch device 68 will be opened, so that the feedback signal will not be affected by the low gain resistive negative feedback circuit 69 (the resistor Rf2 and the capacitor Cf2) and be fed back from the output port 66 to the input port 62 mainly via the high gain resistive negative feedback

circuit 67. In the low-gain mode, due to that most of the input signal SI3 will pass the transistors Q7, Q9 to the voltage source VCC, in order to process the signal fed back via the voltage source VCC, the switch device 68 will be closed so that most of the feedback signal is fed back from the voltage source VCC to the input port 62 via the low gain resistive negative feedback circuit 69. Therefore, by properly determining the values of the resistor Rf2 and the capacitor Cf2, the input impedance Zin3 (of the amplifier 60) can remain substantially fixed in both the low-gain mode and the high-gain mode for avoiding affecting the performances of the filter.

[0031] Please notice that the types of the transistors Q7-Q11 in the above-mentioned embodiment can be bipolar junction the transistors (BJT) or metal-oxide semiconductor (MOS) transistors. Please refer to Fig.6, which is a schematic diagram of another embodiment showing an amplifier 80 according to the present invention. Inheriting the characteristics of the former embodiment shown in Fig.5, the amplifier 80 of the present embodiment also includes an input port 82 (for receiving an input signal SI3), a gain circuit 84, and an output port 86. In addition, the amplifier 80 includes an input impedance Zin3. The gain circuit 84

consists of transistors Q7'-Q11', three adjustable biases B4'-B6', a high gain resistive negative feedback circuit 87 (including a resistor Rf1' and a capacitor Cf1'), and a low gain resistive negative feedback circuit 89 (including a resistor Rf2' and a capacitor Cf2'). The main difference between the present embodiment and the embodiment shown in Fig.5 is that the two resistive negative feedback circuits in the present embodiment are installed with switch devices, a first switch device 83 electrically connected to the high gain resistive negative feedback circuit 87 and a second switch device 85 electrically connected to the low gain resistive negative feedback circuit 89. The first switch device 83 can be implemented by a transistor Q12 and a control signal Ctr1, and the second switch device 85 can also be implemented by a transistor Q13 and a control signal Ctr2. The second switch device 85 can correspond to the switch device 68 in the embodiment shown in Fig.5. Therefore, in the high-gain mode, the second switch device 85 is opened, and the first switch device 83 is closed so that the feedback signal can be fed back from the output port 86 to the input port 82 totally via the high gain resistive negative feedback circuit 87. On the other hand, in the low-gain mode, the first switch de-

vice 83 is opened, and the second switch device 85 is closed so that the feedback signal can be fed back from the voltage source VCC' to the input port 82 totally via the low gain resistive negative feedback circuit 89. Similarly, by properly determining the values of the resistor Rf1', the capacitor Cf1', the resistor Rf2', and the capacitor Cf2', the input impedance Zin3' of the amplifier 80 can remain substantially fixed in the low-gain mode and the high-gain mode.

[0032] In fact, the number of gain mode is not limited to just two: "high" and "low". Regarding the embodiment shown in Fig.6, when being implemented, the bias B5' can bekept at a predetermined voltage value, while the bias B6' is switched among three different voltages respectively higher than, low than, or equal to the bias B5' to achieve the transformation among three different gain modes. Please refer to Fig.7, which is a schematic diagram of a detailed embodiment shown in Fig.6. In order to emphasize the switch among three different voltages corresponds to the transformation among three different gain modes, the embodiment shown in Fig.7 shows detailed circuitries of the three adjustable biases B4'-B6'. The three biases B4'-B6' respectively correspond to the three bias

suppliers 90, 91, 92. The bias B5' is substantially fixed at a predetermined voltage value, and the predetermined voltage value is shown in Fig.8, which is a list illustrating the three biases B4'-B6' shown in Fig.7. As shown in Fig.8, the predetermined voltage value of the bias B5' is 1.6, and the bias B6' can be switched between a high voltage value (2.7V) and a ground voltage GND (0V) to switch the amplifier 80 between the low-gain mode and the high-gain mode. When the bias B6 is totally the same as the bias B5' (1.6V), among the input signal SI3, the amount delivered from the transistors Q10', Q11' to the output port 86 is similar to that delivered from the transistors Q7', Q9' to the voltage source VCC'. Therefore, the gain ratio is located between the gain ratio in the high-gain mode and that in the low-gain mode; the situation is called a medium-gain mode. In the medium-gain mode, the first switch device 83 and the second switch device 85 both conduct so that the input impedance Zin3' of the amplifier 80 in the medium-gain mode remains the same as that in the high/low-gain mode. Therefore, the amplifier 80 operating in the three different gain modes (high, low, and medium) has a substantially fixed input impedance Zin3'. In addition, the number of the gain modes is not re-

stricted to a certain number; that is, the main characteristic of the present invention is utilizing a plurality of resistive negative feedback circuits, which are installed with corresponding switch devices and located in a plurality of paths the feedback signal passes in various gain modes, to respectively process the feedback signal in various gain modes in order to keep the input impedance of the amplifier substantially fixed in various gain modes.

[0033] Please notice that the above-mentioned embodiments of amplifiers shown in Fig.5 to Fig.7 are mainly applied in the receiver of a wireless communications system to be a low-noise amplifier. In summary, the method of the present invention for keeping the input impedance of the amplifier substantially fixed in a plurality of gain modes can refer to Fig.9, which is a flow chart showing a method embodiment according to the present invention. The amplifier includes an input port, a gain circuit, at least a switch device, a plurality of resistive negative feedback circuits, and an output port. The present invention includes following steps:

[0034] Step 100: utilize the input port to receive an input signal;

[0035] Step 102: utilize the gain circuit to amplify the input signal by a corresponding gain ratio in each gain mode;

[0036] Step 104: utilize the plurality of resistive negative feedback circuits and at least a switch device to keep the input impedance of the amplifier substantially fixed in various gain modes. In detail, operate at least a switch device to make the feedback signal feed back through at least a corresponding resistive negative feedback circuit to the input port in various gain modes, so that the input impedance of the amplifier remains substantially fixed in various gain modes;

[0037] Step 106: utilize the output port to output the input signal amplified by the gain circuit.

[0038] Another main characteristic of the present invention is the characteristic of a differential amplifier. The differential amplifier of the present invention can be implemented by merging two amplifiers shown in Fig.5 to Fig.7, and wherein one of the two amplifiers is treated as a positive amplifier circuit while the other as a negative amplifier circuit. The output signal is a difference between the two output signals of the two amplifiers. Please refer to Fig.10, which is a functional block diagram of a differential amplifier 100 according to the present invention. The differential amplifier 100 includes a positive input port 102P, a negative input port 102N, a positive amplifier cir-

cuit 100P, a negative amplifier circuit 100N, a positive output port 106P, and a negative output port 106N. The differential amplifier 100 further includes an input impedance ZinD. The positive input port 102P is used to receive a positive input signal SIP, and the negative input port 102N is used to receive a negative input signal SIN. The positive amplifier circuit 100P is electrically connected to the positive input port 102P, and the negative amplifier circuit 100N is electrically connected to the negative input port 102N. In addition, the positive output port 106P is electrically connected to the positive amplifier circuit 100P in order to output the positive input signal SIP processed by the positive amplifier circuit 100P; the negative output port 106N is electrically connected to the negative amplifier circuit 100N in order to output the negative input signal SIN processed by the negative amplifier circuit 100N. Actually, the positive input port 102P, the positive amplifier circuit 100P, and the positive output port 106P can be combined to be regarded as a disclosed low-noise amplifier (shown in Fig.5 to Fig.7) according to the present invention. Similarly, the negative input port 102N, the negative amplifier circuit 100N, and the negative output port 106N can also be combined to be regarded as an

(low-noise) amplifier. Please refer to Fig.11, which is a schematic diagram of a detailed embodiment ofthe differential amplifier 100 shown in Fig.10, and the embodiment shown in Fig.11 is implemented by merging the two amplifiers 80 shown in Fig.6. The differential performance of the differential amplifier depends on the accuracy of the phase difference between the positive input signal and the negative input signal. When the phase difference is not accurate, a common mode signal will emerge to affect the differential performance. As shown in Fig.11, the positive amplifier circuit 100P includes a positive gain circuit 104P, a plurality of (two) positive resistive negative feedback circuits 110P, and a plurality of (two) positive switch devices 108P. The positive gain circuit 104P is used to amplify the positive input signal SIP by a corresponding gain ratio for in each gain mode, and the plurality of positive resistive negative feedback circuits 110P and the positive switch devices 108P can be used to keep the input impedance ZinP of the positive amplifier circuit 100P substantially fixed in various gain modes. The negative amplifier circuit 100N operates the same as the positive amplifier circuit 100P does.

[0039] According to the preceding paragraph, the positive ampli-

fier circuit 100P and the negative amplifier circuit 100N have substantially fixed input impedances in various gain modes. Therefore, we can implement the positive amplifier circuit 100P and the negative amplifier circuit 100N with two identical amplifiers so that the input impedance of the positive amplifier circuit 100P is equal to that of the negative amplifier circuit 100N in various gain modes (ZinP = ZinN). Due to that the input impedance ZinD of the differential amplifier 100 is a mathematical combination of the input impedance ZinP and the input impedance ZinN, the input impedance ZinD of the differential amplifier 100 can remain substantially fixed in various gain modes. That is, if each amplifier contained in the differential amplifier 100 has the substantially fixed input impedance, the input impedance ZinD of the differential amplifier 100 will remain substantially fixed. In addition, since the differential amplifier 100 operates in the differential mode, the differential amplifier 100 has more advantages than do general single-ended amplifiers, such as the embodiments shown in Fig.5 to Fig.7. With the characteristics of the differential mode, the differential amplifier 100 can get rid of being interfered and generating interference, generating less $2^{nd}$ order interception point

(IP2) in the front-end of the receiver with less DC offset. In addition, the frequency response of the differential amplifier 100 is wider than that of general single-ended amplifiers. Being a low-noise differential amplifier, the differential amplifier of the present invention can be applied to a wireless communications system.

[0040] According to the present invention, an amplifier with substantially fixed input impedance is disclosed. In the amplifier, a plurality of resistive negative feedback circuits are respectively installed in a plurality of corresponding paths through which a feedback signal will pass in various gain modes. In each gain mode, at least a corresponding resistive negative feedback circuit will be used to process the corresponding feedback signal, so that the input impedance of the amplifier can remain substantially fixed in various gain modes. Therefore, the distortion of a filtering response caused by impedance mismatch can be avoided. In addition, a differential amplifier with substantially fixed input impedance is also disclosed to meet various requirements in communications systems.

[0041] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accord-

ingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.